



Identity

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Born 19 august 1982

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Work

- ▶ Software Developer in the Software Tools Division section of **Kalray**,
Montbonnot-Saint-Martin. Mar. 2010–Mar. 2013
- ▶ Post-Doctoral fellow at the **Indian Institute of Science** (IISc) of Bangalore, India,
at the Supercomputer Education and Research Center on GPGPU. 2009

Education

École Normale Supérieure de Lyon

- Ph.D. Thesis, graduated *with highest honors* (graduated on **April 30th 2009**)
- ▶ “A Study of Spilling and Coalescing in Register Allocation as Two Separate Phases”
 - ▶ Advisors: Fabrice RASTELLO and Alain DARTE
 - ▶ Area of Study: program compilation

Master in Computer Science (*Informatique Fondamentale*) at ÉNS Lyon 2005

Teaching

Courses

- ▶ C project, ENSIMAG (1a), Grenoble scheduled Jun. 2013
- ▶ Algorithm Design, Master MoSIG, IMAG, Grenoble Sept.-Nov. 2012
- ▶ Algorithms 2, ENSIMAG (1a), Grenoble 2011–2013

Invited talks

- ▶ Vignan University, India: on general computer science and GPGPU Nov. 2009
- ▶ Delaware University, USA, Part 5 of LCPC tutorial on SSA Oct. 2009
- ▶ IISc of Bangalore, India: two lectures on “*advanced register allocation*” Apr. 2009

As a teaching assistant at École Normale Supérieure de Lyon

- ▶ Parallel algorithms (Master 1) 2008–2009
- ▶ Programming (License 3) and Compilation (Master 1) 2007–2008
- ▶ Algorithms (License 3) and Compilation (Master 1) 2006–2007

Lycée du Parc, Lyon

- ▶ Teaching Turbo Pascal to first year HEC students (commercial studies) 2004–2006

Internships

- Master 2, with F. Rastello: complexity study of the spill problem under SSA 2005
- Master 1, University of Michigan (USA), with Scott Mahlke about Streams in Custom Processors summer 2004
- License 3, with F. Rastello, on Optimization of Instruction Cache summer 2003

Publications

Journals:

- ▶ “Procedure placement using temporal-ordering information: dealing with code size expansion” in *Journal of Embedded Computing* (2005)

Conferences:

- ▶ “Parallel Copy Motion” at *SCOPES’10*
- ▶ “Advanced conservative and optimistic coalescing” at *CASES’08*
- ▶ “On the complexity of register coalescing” at *CGO’07 (best paper award)*
- ▶ “On the complexity of spill everywhere under SSA form” at *LCTES’07*
- ▶ “Register allocation: What does the NP-Completeness proof of Chaitin et al. really prove?” at *WDDD’06* and *LCPC’06*
- ▶ “Procedure placement using temporal-ordering information: dealing with code size expansion” at *CASES’04*

Workshops:

- ▶ “A Tirex-based SSA interpreter” at *DCE’12 (HiPEAC)*
- ▶ “Tirex: A Textual Target-Level Intermediate Representation for Compiler Exchange” at *WIR’11 (CGO)*

Events

- ▶ Organization of WIR’11: Workshop on Intermediate Representation at CGO’11
(Chair, with S. Hack and E. Visser)
- ▶ Examiner at Boubacar Diouf’s Ph.D. defense

Apr. 2011
Dec. 2011

Skills

Programming: C, Pascal, Perl, Ruby, OCaml, *T_EX/L^AT_EX*.
Work environment: Linux
Languages: *French* (mother tongue) and *English* (fluent)